Tri-national Workshop in Micro & Nano Technology
Macedonia, Bulgaria and Switzerland
14-18 May 2012

at

Ss Cyril and Methodius University Skopje
Faculty of Electrical Engineering and Information Technology

Tri-national MNT Workshop
Macedonia, Bulgaria & Switzerland
14-18 May 2012 - Skopje

Organisation Committee

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The organisation committee acknowledges financial support by the Swiss National Science Foundation

Institut de Micro et Nano Techniques
heig-vd
Haute Ecole d'Ingénierie et de Gestion du Canton de Vaud
FNSNF
Fonds national suisse de la recherche scientifique

Workshop programme

	14.05.2012	15.05.2012	16.05.2012	17.05.2012	18.05.2012
	Monday	Tuesday	Wednesday	Thursday	Friday
08:00 - 09:00	Arriving of the workshop participants	Breakfast & transport to FEEIT	Breakfast & transport to FEEIT	Breakfast & transport to FEEIT	Breakfast
09:00 - 10:30		Workshop opening, Dean of FEEIT, Prof. Schintke, Participant introduction Session Tu1	Session W1	Session Th1	Participants departure
10:30 - 11:00		Coffee break	Coffee break	Coffee break	
11:00 - 12:30		Session Tu2	Session W2	Session Th2, discussion & closing	
12:30 - 14:30		Lunch	Lunch	Excursion	
14:30 - 16:00		Session Tu3	Technical visit (Plasma technology center)		
16:00 - 16:30		Coffee break			
16:30 - 17:30		Visit of FEEIT facilities			
		Dinner		Night in the city	
20:00 -	Welcome reception		Free evening		

Presentations

Tuesday, 15 May 2012

Session Tu1:

Nanocomposite Solar Cells: Possible Low-Cost Alternative to Silicon,
Prof. Dr. Hristina SPASOVSKA (FEEIT - Macedonia)

The low-cost photovoltaic solar cells are considered as a promising technology having the potential to significantly decrease the costs of solar energy. They have attracted considerable interest on the scientific and production community due their low-energetic production cost and low-cost of the raw materials, which offer the perspective of very low-cost fabrication and present attractive features that facilitate market entry. The phenomenal progress realized recently in the fabrication and characterization of nanocrystalline materials has opened up vast new opportunities for these systems.
A possible alternative, which allows the use of low-quality materials, are 3D solid-state solar cells. These cells are comprised of an interpenetrating network of n-type and p-type semiconductors on a nanometric scale. In this type of solar cells, CuInS2 (CIS) is used both as light absorber and hole transport layer, and is deposited inside the pores of mesoporous film of TiO2.
Our investigations are focused on 3D solid-state nanocomposite solar cells which include several thin film layers on glass substrate: FTO conducting layer; TiO2 compact film (100–200 nm); TiO2 nanocrystalline film (2–10 □m); In2S3 intermediate layer (~ 60 nm) and CuInS2 film (500–1000 nm).

The obtained results show that the structural parameters of all thin layers are directly connected with concentration of precursor solution, temperature of the substrate and duration of spray deposition. Investigations of the films were made by Raman, UV-VIS Spectroscopy, SEM and AFM.

Tuesday 15 May 2012
Session Tu2:

Ultrasonic nanowelding
Arvydas LITVINAS (HEIG-VD, Telsonic - Switzerland)

Telsonic is a leading company in the field of ultrasonic industrial applications.(http://www.telsonic.com)

Working as an Engineer at SKAN AG
Olivera SCHEUBER (HEIG-VD, SKAN AG - Switzerland)

The 1968 founded SKAN AG, belongs to the pioneer companies in the special area of cleanroom equipment and construction of Isolators for the pharmaceutical chemical industry. (http://www.skan.ch)

Tuesday 15 May 2012
Session Tu3:

Optical and Structural Properties of TiO2 Nanostructures
Tanja IVANOVSKA (FEEIT-Macedonia)

The dye-sensitized solar cells (DSSC) are the most serious concept that could replace the silicon solar cells. These are low-cost photovoltaics, and represent a technology which could seriously decrease the cost of the electrical energy they produce.
The dye-sensitized solar cells are composed of several layers of materials that belong to the group of inorganic semiconductors. In recent years the scientific community has taken a great interest in TiO2 nanostructures, especially TiO2 nanocrystalline films that have proven to be irreplaceable as photoelectrodes in the DSSC. The optical and structural characteristics of the nanocrystalline films are significant for the cell operation and high efficiency. The film properties directly depend on the chemical composition of the solution used for deposition. Therefore optimization of the parameters such as: crystal structure of the films, surface uniformity, thickness, particle size and porosity, is crucial. The optical and structural analysis and characterization of the films can be done with several characterization techniques like the optical spectroscopy in the visible and ultraviolet spectral region (UV-Vis), Raman spectroscopy and atomic force microscopy (AFM).

Wednesday, 16 May 2012

Session W1:

Scanning Probe Microscopy in R&D: methods & application examples from photovoltaics, organic and molecular electronics

Prof. Dr. Silvia Schintke (HEIG-VD, Institut MNT - Switzerland)

MNT-LANS - Institute of Micro & Nano Technics - Laboratory of Applied NanoSciences is an R&D unit of HEIG-VD, University of Applied Sciences Western Switzerland. Its R&D activities focus on the characterisation of nano- and microstructured surfaces and materials for industrial applications, e.g. in the fields of photovoltaics, microelectronics, thin film coatings, anti-corrosion layers, or medical implants. (http://www.heig-vd.ch; http://www.mnt-lans.ch).
This talk gives examples on Scanning Probe Microscopy Applications in the field of photovoltaics, ultrathin oxides, as well as organic and molecular electronics.

Experience from R&D laboratory experiments in NMT training

Jerôme BORBOËN (HEIG-VD, HE-Arc Institut de Micro & Nanotechniques Appliquées - Switzerland)

Examples and experience from the Swiss Master of Advanced Studies in Nano & Micro Technology (www.nanofh.ch/nmt-master)

Session W2:

Simulation of Self-Heating Effects in Nanoscale SOI Devices and Nanowire Transistors

Prof. Dr. Katerina RALEVA (FEEIT - Macedonia)

The problem of heat and degradation of device characteristics has been an issue that is well known to the power electronics community. With applied voltages of over 40 V, carriers occupy states very high in the energy and transfer it to the lattice, mainly through the interactions with optical phonons. Power devices are typically large in size and drift-diffusion model for the electron and hole transport coupled with a heat conduction model, in which a Joule heating term is used, has been extensively used to model the behavior of these devices. In few instances hydrodynamic model has been used for modelling of the carrier (electrons and holes) transport. For digital circuits operated at much lower voltages, self-heating (that manifests itself in a mobility degradation at high current densities) has been much less of a problem as in conventional Si MOSFETs because the silicon body has very large thermal conductivity and most of the heat is dissipated through the substrate. The problem arises in Silicon On Insulator (SOI) devices (fully-depleted (FD) SOI devices, partially-depleted (PD) SOI devices, FinFETs, dual-gate (DG) structures) which are supposed to replace conventional MOSFET devices beyond the 22 nm technology node. There are several problems associated with SOI technology. First, SiO2 is a very bad thermal conductor as the thermal conductivity of SiO2 is about 100 times smaller than that of silicon. Second, silicon film has thermal conductivity smaller than bulk Si because of the fact that the phonon mean free path in Si is very large and phonon boundary scattering reduces the thermal conductivity below its bulk value. The reduction of the thermal conductivity is even more pronounced in silicon nanowires because of the stronger boundary scattering.
In this talk a five years of work on modelling self-heating effects in nanoscale devices at Arizona State University (ASU) will be summarized. The key features of the electro-thermal Monte Carlo device simulator (the two-dimensional and the three-dimensional version of the tool) will be presented and then series of representative simulation results that clearly illustrate the importance of self-heating in larger nanoscale devices made in silicon on insulator technology (SOI) will be discussed. The simulation results also show that in the smallest devices considered, the heat is in the contacts, not in the active channel region of the device. Therefore, integrated circuits get hotter due to larger density of devices but the device performance is only slightly degraded at the smallest device size. This is because of two factors: pronounced velocity overshoot effect and smaller thermal resistance of the

buried oxide layer. Efficient removal of heat from the metal contacts is still an unsolved problem and can lead to a variety of non-desirable effects, including electromigration.

Thursday, 17 May 2012

Session Th1:

Application of High-K Dielectrics in Nanotechnologies

MSc. Lihnida STOJANOVSKA GEORGIEVSKA (FEEIT-Macedonia)

Since the advent of the metal-oxide semiconductor (MOS) system over 40 years ago, the SiO2 gate oxide has been serving as the key enabling material in scaling silicon CMOS technology. However, continued SiO2 gate oxide scaling is becoming exceedingly difficult since (a) the gate oxide leakage is increasing with decreasing SiO2 thickness, and (b) SiO2 is running out of atoms for further scaling. As Moore's law extends scaling and device performance into the 21st century, high-κ gate dielectrics and metal gate electrodes will be required for high-performance and low-power CMOS applications in the 45 nm node and beyond. Here a brief description of the choice of high-k materials and the methods of their fabrication and characterization will be given.

Optional: Tribology in Watchmaking Industry

Jerôme BORBOËN (HEIG-VD, HE-Arc Institut de Micro & Nanotechniques Appliquées - Switzerland)

Session Th2:

Thermal management of microelectronic devices and circuits

Prof. Dr. Slavka Tzanova (TU Sofia, Bulgaria)

This talk gives an overview on concepts and recent achievements in the thermal management of microelectronic devices and circuits.

- Excursion and END – The next tri-national workshop in 2013 or 2014 will be defined -